Effects of Package Level Structure and Material Properties on Solder Joint Reliability Under21,, T7/0.TE.54i2.7(L)8.5 [(52)

JESD22-B111 is conducted to obtain the com
mode, rate, location, and the corresponding bo
accelerations. Finite element models are develop
against the experimental results. For a CS BG
compliance of the plastic substrate/mold compo
ìstress buffer mechanismî at corner joints in
stresses. For a copper post (or pillar) WLP, wa
which encapsulates copper pillars, serves as a
for solder joint stress reduction under dynamic
prehensive data from simulation and experimen
that package structure and material properties pla
role on the dynamic responses of solder joints. T
joint reliability performance of a CS BGA or
depends on the resultant effects of package str
properties, package body size, and the compone

***Index Terms*—Ball grid array (BGA),
dynamics, finite element analysis (FEA), impac
B111, reliability, solder joints, wafer level pac**

I. INTRODUCTION

CBGA packages, which usually apply for wire-bond devices, are defined for the package/die size ratio less than 1.2. Conventional (fan-in) WLPs [1], on the other hand, are a unique form of packages and have the distinction of being truly die-sized, not "CS." They are formed on the dies while they are still on the uncut wafer. There have been a variety of WLP technologies with distinct package structures. Standard ball on I/O WLP has evolved with the incorporation of redistribution layer (RDL) process, copper-post process, and compliant layer process [2], [3].

A mechanical impact resulting from mishandling, such as being dropped during transportation or customer usage, may cause solder joint failures of these packages. A board level drop test method, JESD22-B111 [4], has been standardized to evaluate the performance of integrated circuit packages under standard drop conditions. Three primary failure modes are often observed in drop test for BGA and WLP packages: copper trace crack or pad crater in printed circuit board (PCB), crack at intermetallic (IMC) layer of solder joints, and die-level cracks, such as in RDL or copper interconnect. Because PCB failures (trace crack or pad crater) provide a misrepresentation of the actual package performance, some board design guidelines have been further recommended and adopted to avoid such failure modes during test [5].

To correlate board level dynamic responses to component failures, a multichannel real-time monitoring system has been applied to obtain board strains and accelerations at various locations of PCB using strain gages and accelerometers [6], [7]. A digital image correlation system integrated with the high speed cameras has also been developed to acquire the images of entire surfaces of dynamic deformation of board [7]. Various shock/impact modeling techniques have

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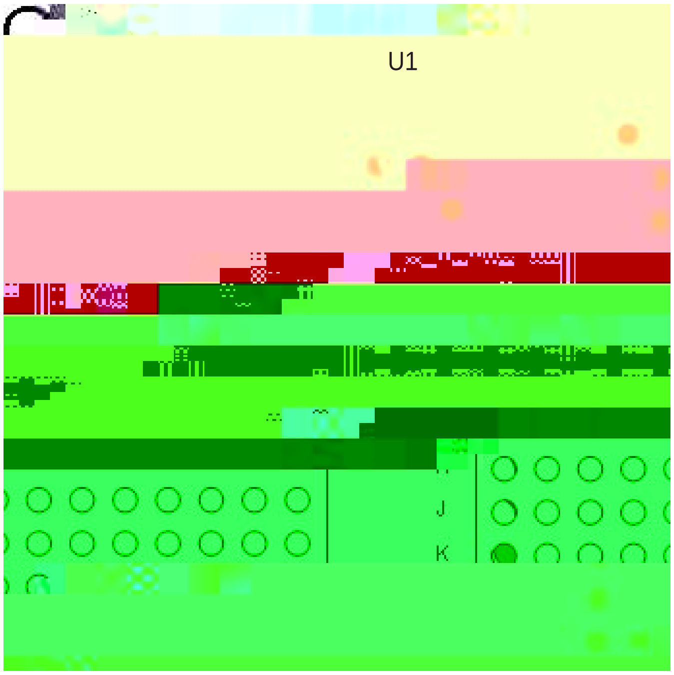


Fig. 4. Crack map of group A WLP after drop test (red areas correspond to solder joint IMC crack at package side).

1500-g peak and 0.5-ms duration, which can be described by equation as follows:

$$a = \begin{cases} 1500g \sin\frac{\pi t}{t_w}, & t \le t_w, t_w = 0.5 \\ 0, & t \ge t_w \end{cases} \qquad (1)$$

where a is the acceleration of the drop table, g is acceleration due to gravity (9.8 m/s^2), and t_w is the impulse duration (ms).

Strain gauge rosettes are used to measure board strain transient responses at various locations. The comparison between the strain measurement and finite element results will be discussed in Section V. Dye and pry techniques are applied for failure analysis for the selected components to determine the failure mode and crack propagation pattern. The dominant failure mode in this study was the solder joint crack at IMC layer on the component side. A typical failure map showing crack size and locations is illustrated in Fig. 4. It is seen that the solder joints at left and right columns show the most crack propagations compared to the other columns. In addition, the cracks initiate from solder joint inner side and propagate toward opposite side.

A typical Weibull plot for the failure rate of all six groups is shown in Fig. 5 for a 6 × 6 mm WLP package. A total of ten test boards were tested to have sufficient failure data points for all groups. For the package size of 6 × 6 mm, the failure rate rank is: A>F>E>B>D>C. It is seen that group A (corner components) has the greatest failure rate, followed by groups F and E (center row components). Groups B, C, and D have the smallest failure rates.

For various types of packages with various sizes, it is generally seen that the first resonant frequency of the test board is registered around 230 Hz, and the second one is found at approximately 650 Hz.

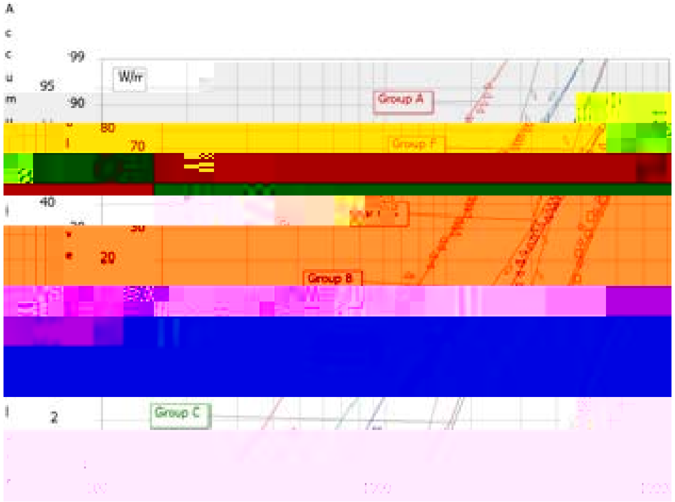
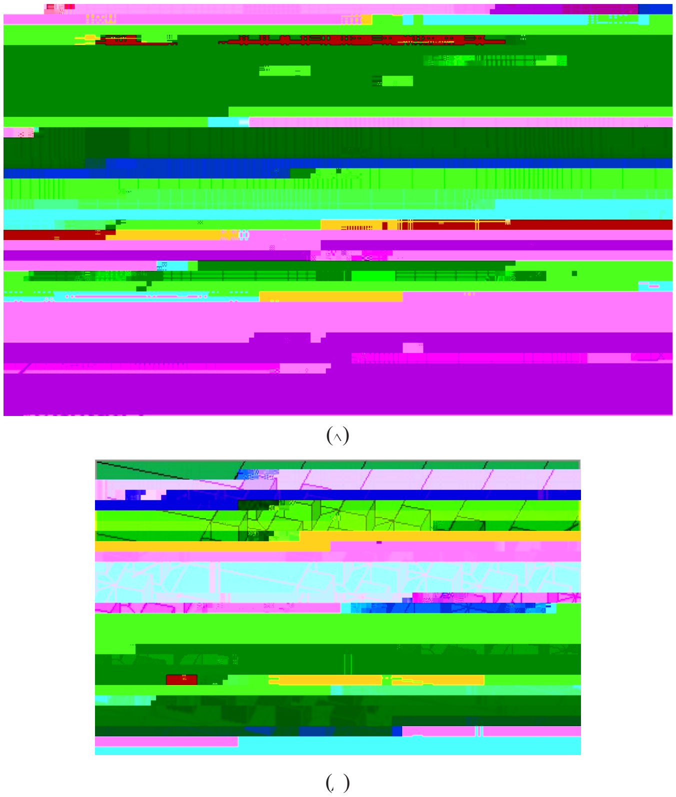


Fig. 5. Weibull plot of drop test failures for six component groups for a 6 × 6 mm copper post WLP.

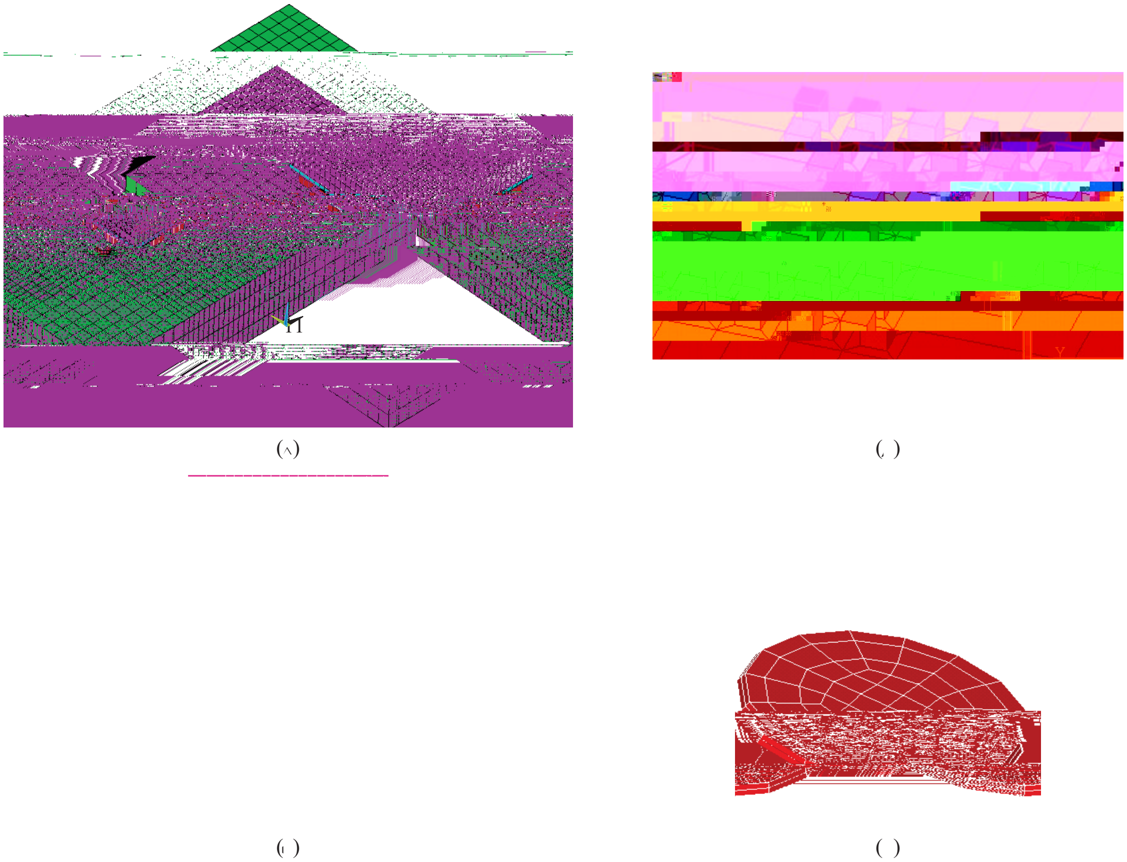

(a)

(b)

Fig. 6. Quarter global finite element model. (a) Global finite element model for board and (b) solder joint finite element mesh in global model.

IV. MATHEMATICAL FORMULATIONS AND FINITE ELEMENT MODELS

For JESD22-B111 drop test, the main interest is the component dynamic responses, especially the solder joint transient stresses. In solving a dynamic problem, it is important to know whether the problem falls into the category of wave propagation or structural transient dynamic response. It may be



(a) (b) (c) (d)

Fig. 7. Local finite element model. (a) Overall local model. (b) Details of solder joint finite element model. (c) Cross-section of refined meshes of corner joints. (d) IMC layer finite element mesh.

helpful to compare the time scale of stress wave propagation in PCB to a typical impulse scale (0.5 ms per JEDEC definition) and PCB dimension. The speed of stress wave is $\sqrt{\mu/\rho}$, where μ and ρ are shear modulus and density of the board. The value is approximately 7×10^3 mm/ms, which means that the stress wave has already traveled back and forth in PCB (∼130-mm length) several times within 0.5 ms to reach an equilibrium of being bulk structural dynamic responses. Therefore, the problem under study is solved by structural dynamics.

For the loading condition described in (1), the load in terms of acceleration on mounting screws can be converted to body

TABLE II

failure. A tradeoff design must be considered in the selection of compliant layer material, such as wafer level epoxy in copper post WLP.

D. Resultant Effects

To compare solder joint performance in a BGA package

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